WHAT IS CLAIMED IS:

1. A PLL circuit including a phase comparator to control an output signal of a variable frequency oscillator, a reference signal of a predetermined frequency is a first input signal, and one of an output signal and a divided signal of the output signal from the variable frequency oscillator is a second input signal,

wherein the phase comparator for comparing the first input signal and the second input signal, comprising:

a generator configured to generate a reset signal at each rising edge or each falling edge of the first input signal;

a counter configured to count the second input signal at each interval determined by the reset signal, a counted value represents a ratio of frequencies of the first input signal and the second input signal; and

a subtractor configured to calculate a difference between the counted value and a set value representing a predetermined ratio of the frequencies of the first input signal and the second input signal.

2. The PLL circuit according to claim 1, further comprising:

an integrator configured to integrate the difference outputted from said subtractor, the integrated value represents a phase difference of the frequencies of the first input signal and the second input signal.

3. A PLL circuit including a phase comparator to control an output signal of a variable frequency oscillator, a reference signal of a predetermined frequency is a first input signal, and one of an output signal and a divided signal of the output signal from the variable frequency oscillator is a second input signal,

wherein the phase comparator for comparing the first input signal and the second input signal, comprising:

a generator configured to generate a load signal at each rising edge or each falling edge of the first input signal; and

a counter configured to count the second input signal at each interval determined by the load signal, to calculate a difference between a counted value and a set value representing a predetermined ratio of frequencies of the first input signal and the second input signal, and to integrate the difference, an integrated value represents a phase difference of the frequencies of the first input signal and the second input signal.

4. A PLL circuit including a phase comparator to control an output signal of a variable frequency oscillator, a reference signal of a predetermined frequency is a first input signal, and one of an output signal and a divided signal of the output signal from the variable frequency oscillator is a second input signal,

wherein the phase comparator for comparing the first input signal and the second input signal, comprising:

a counter configured to count the second input signal at each rising edge or each falling edge of the first input signal, to calculate a difference between a counted value and a set value of an integer part of a predetermined ratio of frequencies of the first input signal and the second input signal, and to integrate the difference as a digital value;

an integrator configured to integrate a set value of a decimal part of the predetermined ratio of frequencies of the first input signal and the second input signal; and

a subtractor configured to calculate a difference between the digital value from said counter and an integrated value from said integrator, the difference represents a phase difference of the frequencies of the fist input signal and the second input signal.

5. A PLL circuit including a phase comparator to control an output signal of a variable frequency oscillator, a reference signal of a predetermined frequency is a first input signal, and one of an output signal and a divided signal of the output signal from the variable frequency oscillator is a second input signal,

wherein the phase comparator for comparing the first input signal and the second input signal, comprising:

a counter configured to count the second input signal at each rising edge or each falling edge of the first input

signal, and to output a counted value as a digital value representing a ratio of frequencies of the first input signal and the second input signal;

a converter configured to convert a non-integer digital set value as a predetermined ratio of the frequencies of the first input signal and the second input signal to a sequence of integer digital values whose average value coincides with the digital set value; and

a subtractor configured to calculate a difference between the counted value output from said counter and the integer digital values output from said converter.

6. The PLL circuit according to claim 5, wherein the non-integer digital set value is comprised of an integer part and a decimal part representing the predetermined ratio of each frequency of the first input signal and the second input signal.

7. The PLL circuit according to claim 6,

wherein the sequence of integer digital values is comprised of the integer part and a next integer repeatedly arranged by a ratio of the decimal part in the digital set value of non-integer.

8. The PLL circuit according to claim 7,

wherein said subtractor correspondingly subtracts each integer in the sequence of digital values from each integer in the counted value.

9. The PLL circuit according to claim 5, further comprising:

an integrator configured to integrate the difference calculated by said subtractor, the integrated value represents a phase difference of the first input signal and the second input signal.

10. The PLL circuit according to claim 9,

wherein the integrated value represents the phase difference between the first input signal and the second input signal in frequency based on the digital set value.

11. A PLL circuit including a phase comparator to control an output signal of a variable frequency oscillator, a reference signal of a predetermined frequency is a first input signal, and one of an output signal and a divided signal of the output signal from the variable frequency oscillator is a second input signal,

wherein the phase comparator for comparing the first input signal and the second input signal, comprising:

a converter configured to convert a non-integer digital set value as a predetermined ratio of frequencies of the first input signal and the second input signal to a sequence of

integer digital values whose average value coincides with the digital set value; and

a counter configured to count the second input signal at each rising edge or each falling edge of the first input signal, to calculate a difference between a counted value and the integer digital values, and to integrate the difference, an integrated value represents a phase difference of the first input signal and the second input signal.

12. The PLL circuit according to claim 11,

wherein the integrated value represents the phase difference between the first input signal and the second input signal in frequency based on the digital set value.